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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 08/798,227 | 02/11/1997 | BRENT KEETH | 660073.587 | 2230 |

27076 7590 09/16/2003

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| EXAMINER | |
|---|---|
| PEIKARI, BEHZAD | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | 28 |

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 08/798,227 | KEETH, BRENT | |
| | Examiner | Art Unit | |
| | B. James Peikari | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *26* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

*Note:* Upon careful review of the application papers and the prosecution history, it became apparent that the heretofore elusive "echo clock signal" was nothing more than a system clock signal, as output by a memory device as a feedback to a controller, which signal had been modified by the skews and phase shifts and delays which inevitably accompany transmission of signals over bus lines and through the elements of a data processing system.

With this in mind, it became evident that the "echo clock signal" was simply a fundamental feedback signal used to continuously correct the timing errors in memory system by sending the feedback (echo) clock signal from the memory device to the memory controller, for comparison with a master clock signal, to identify any difference between the two and to produce a corrected (revised) timing signal.

This is not an oversimplification of the claims – with this understanding of "echo clock signal", the claims actually become quite broad, to the extent that they would have been taught by a number of prior art systems, only some of which are recited below.

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Pricer, U.S. 5,673,005, or Stephens, Jr. et al., U.S. 5,550,783, or Shimizu et al., U.S. 5,229,929, or Hopkins, U.S. 5,182,524, or Girmay, U.S. 5,130,565, or Furuhata et al., U.S. 4,746,996.

(1) Pricer teaches the concept which is fundamental to the invention, providing an input master clock signal (via input 16), a delayed clock signal which is a modified version of the master clock signal (via output 17) and comparison means (12) to compare the two signals and provide a feedback of the "sensed difference" (13) to provide a continuous correction.

Pricer does not specifically mention that this feedback loop may occur between a memory device and a memory controller, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize it in such a system, since it would continuously minimize or even eliminate the errors which would otherwise have been caused by the inevitable propagation delays in such a memory system.

(2) Stephens, Jr. et al. teach the use of an input master clock signal (the "external clock signal" a.k.a. $CLK_{SYS}$) and a delayed clock signal which is a modified version of the master clock signal (the "delayed internal clock signal") and a comparator (138) to compare the two and to provide a feedback (via the "feedback circuit") from the SRAM (110) to its controller (122).

Stephens, Jr. et al. do not specifically mention the "echo clock signal" *by name*, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that the "delayed internal clock signal" of Stephens, Jr. et al. is identical to the "echo clock signal" of the present claims, since both are generated to provide continuous feedback for error detection and subsequent correction in a memory system.

(3) Shimizu et al. teach the concept which is fundamental to the invention, providing an input master clock signal ("sine wave reference signal ... generated by the sine wave generator 14"), a delayed clock signal which is a modified version of the master clock signal (provided to *both* elements 13 and 15, for the reasons described below) and comparison means (first by detecting circuit 13 and again by differential amp 17) to compare the two signals and provide a feedback of the "sensed difference" to provide a continuous correction (note the corrected signal from differential amp 15 and double corrected by differential amp 17).

Shimizu et al. teach a "double correction" because it corrects for distortion in the waveform of the "engine generator" output voltage as well as for the peak value of the reference frequency according to the AC output current. Note columns 7 and 8.

Shimizu et al. does not specifically mention that this feedback loop may occur between a memory device and a memory controller, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize it in such a system, since it would continuously minimize or even eliminate the

errors which would otherwise have been caused by the inevitable propagation delays in such a memory system.

(4) Hopkins teaches providing an input master clock signal (38), a delayed clock signal which is a modified version of the master clock signal (a combination of $V_{ref}$, $V_{out}$ and the trigger signal) and comparison means (34) to compare the two signals and provide a feedback of the "sensed difference" (from elements 34 and 33) to provide a continuous correction.

Hopkins does not specifically mention that this feedback loop may occur between a memory device and a memory controller, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize it in such a system, since it would continuously minimize or even eliminate the errors which would otherwise have been caused by the inevitable propagation delays in such a memory system.

(5) Girmay teaches providing an input master clock signal ("exact duty cycle"), a delayed clock signal which is a modified version of the master clock signal ("the output of a current-controlled pulse width modulator") and comparison means (26) to compare the two signals and provide a feedback of the "sensed difference" to provide a correction. Note columns 2 and 3.

Girmay does not specifically mention that this feedback loop may occur between a memory device and a memory controller, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize it in such a system, since it would continuously minimize or even eliminate the errors which would

otherwise have been caused by the inevitable propagation delays in such a memory system.

(6) Furuhata et al. teach the use of an input master clock signal (note the frequency of the "reference clock", $f_0$.) and a delayed clock signal which is a modified version of the master clock signal (actually, two frequency-divided signals input to comparator 410) and a comparator (410) to compare the two and to provide a feedback (i.e., the amount of the difference) from the memory (2) to its controllers (500 and 600) via compensation circuit 412, which provides continuous correction.

Furuhata et al. do not specifically mention the "echo clock signal" *by name*, however it would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that the "delayed internal clock signal" of Furuhata et al. is identical to the "echo clock signal" of the present claims, since both are generated to provide continuous feedback for error detection and subsequent correction in a memory system.

***Response to Request for Reconsideration***

3. The request for reconsideration filed on July 30, 2003 has been carefully considered. The examiner does not have a written record of the interview held on February 26, 2003, so applicant's summary is especially appreciated.

The examiner has carefully considered applicant's comments, but upon further review of the previous rejection and the claim language, it has been determined that at

least some of the references cited *do* in fact teach a feedback signals transferred between a memory controller and a memory. Note, e.g., Stephens, Jr. et al.

For those references that do not explicitly recited the use of a memory controller, the corresponding rejections provide a carefully reasoned statement of motivation to utilize the prior art systems in a memory controller / memory feedback system.

Consequently, the rejections are maintained from the previous Office action. Any inconvenience to applicant is sincerely regretted and, accordingly, this Office action is being made non-final although the grounds of rejection have not changed.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824.

The examiner generally works alternate weekdays between 11:00 am and 9:00 pm, EST, and on weekends.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

December 15, 2002